LISTING OF CLAIMS:

1. (Currently Amended) A digital test module for testing a phase locked loop circuit, the module comprising:

phase detection means for performing phase measurements of the phase locked loop circuit, wherein the phase detection means comprises:

a reference clock path having first delay means,

a first latch means coupled to receive a reference clock signal from the phase locked loop circuit,

a feedback clock path having second delay means, and

a second latch means coupled to receive a feedback clock signal from the phase locked loop circuit, wherein the first latch means is latched by the feedback clock signal and the second latch means is latched by the reference clock signal;

analogue test means for testing at least one analogue element of the phase locked loop circuit;

frequency measurement means for performing frequency measurements of the phase locked loop circuit; and

means for performing calibration and jitter measurements.

2. (Original) A system comprising the module of claim 1 and the phase locked loop circuit integrated in a single device.

3. (Canceled).

4. (Currently Amended) The module of claim [[3]] 1, wherein the first and the second delay means each comprise a series of delay blocks, each delay block being formed by four inverters.

5. (Original) The module according to claim 1 wherein

the means for performing calibration and jitter measurements includes a multiplexer arranged to receive the reference clock signal and a doubled reference clock signal from the phase locked loop circuit.

6. (Original) The module of claim 5 wherein the means for performing calibration and jitter measurements includes a series of delay blocks arranged as a ring circuit, each of the delay blocks providing a delayed output to a decoder.

7. (Original) The module of claim 6 wherein each of the delay blocks is formed by four inverters.

8. (Currently Amended) ~~The module according to claim 1~~ A digital test module for testing a phase locked loop circuit, the module comprising:
phase detection means for performing phase measurements of the phase locked loop circuit;
analogue test means for testing at least one analogue element of the phase locked loop circuit,
wherein the analogue test means comprises:

a test controller arranged to perform testing of the at least one analogue element;
a first digital-to-analogue converter coupled to the test controller and arranged for providing a first analogue output; and
a second digital-to-analogue converter coupled to the test controller and arranged for providing a second analogue output, wherein the first and second analogue outputs are used in combination to test the at least one analogue element[[.]];

frequency measurement means for performing frequency measurements of the phase locked loop circuit; and
means for performing calibration and jitter measurements.

9. (Original) The module of claim 8 wherein the first analogue output is substantially constant.

10. (Canceled).